Refine Search

Search Results -

Terms	Documents
(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy) same (FIFO or buffer)	63

Database:
US Pre-Grant Publication Full-Text Database
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Search: L1

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, November 02, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy) same (FIFO or buffer)	63	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy) same (FIFO or buffer)	3

Database:
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Search: L2

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, November 02, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy) same (FIFO or buffer)	3	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy) same (FIFO or buffer)	63	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(707/201 |370/401 |370/402 |709/213 |709/214 |709/253 |710/306 |710/312 |710/112 |711/141 |711/148).ccls.	7242

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
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Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, November 02, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	710/306,312,112;711/141,148;709/213,214,253;370/401-402;707/201.ccls.	7242	L3
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy) same (FIFO or buffer)	3	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy) same (FIFO or buffer)	63	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L1 and L3	16

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
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IBM Technical Disclosure Bulletins

Search: L4

Refine Search | Recall Text | Clear | Interrupt

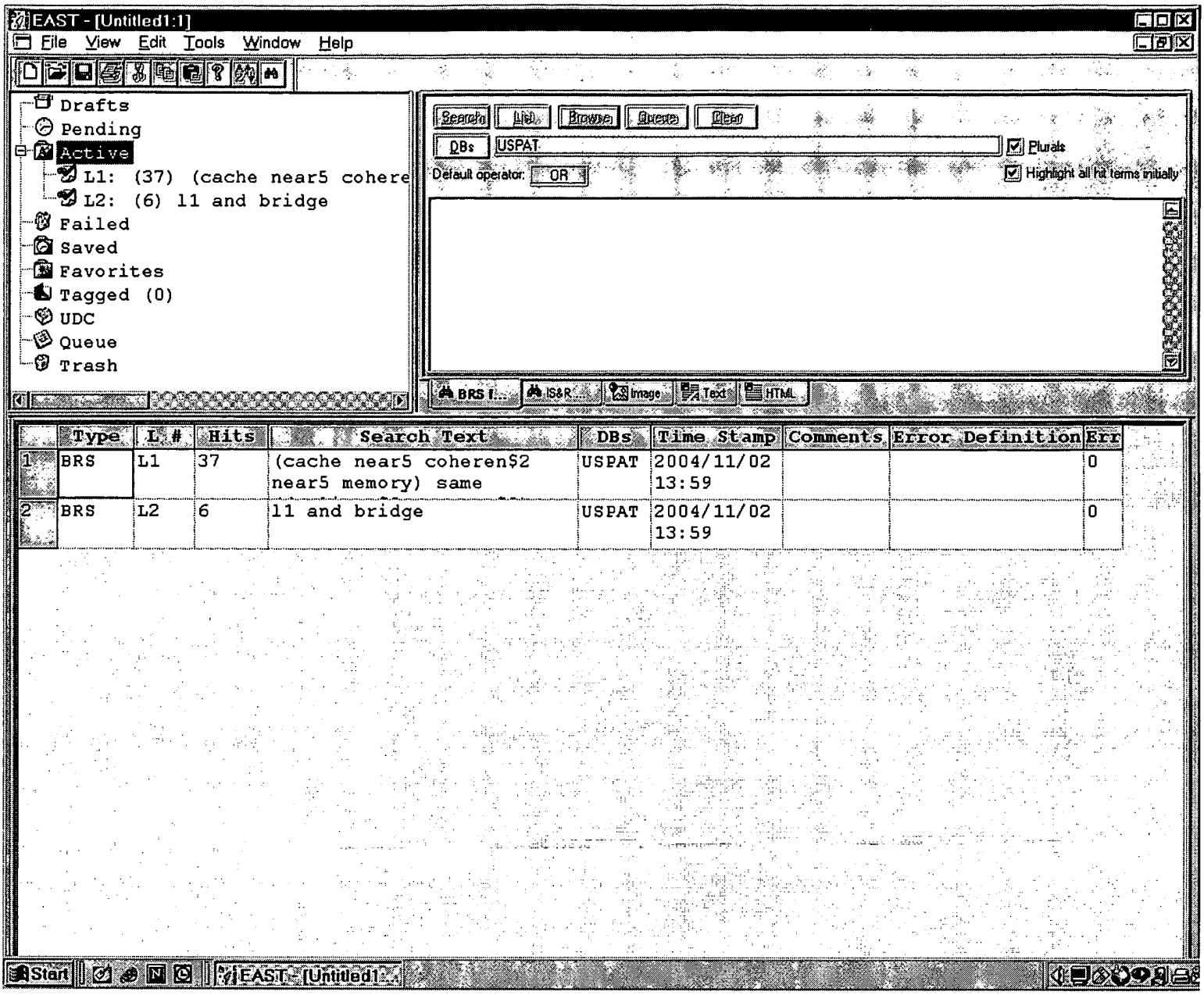
Search History

DATE: Tuesday, November 02, 2004 Printable Copy Create Case

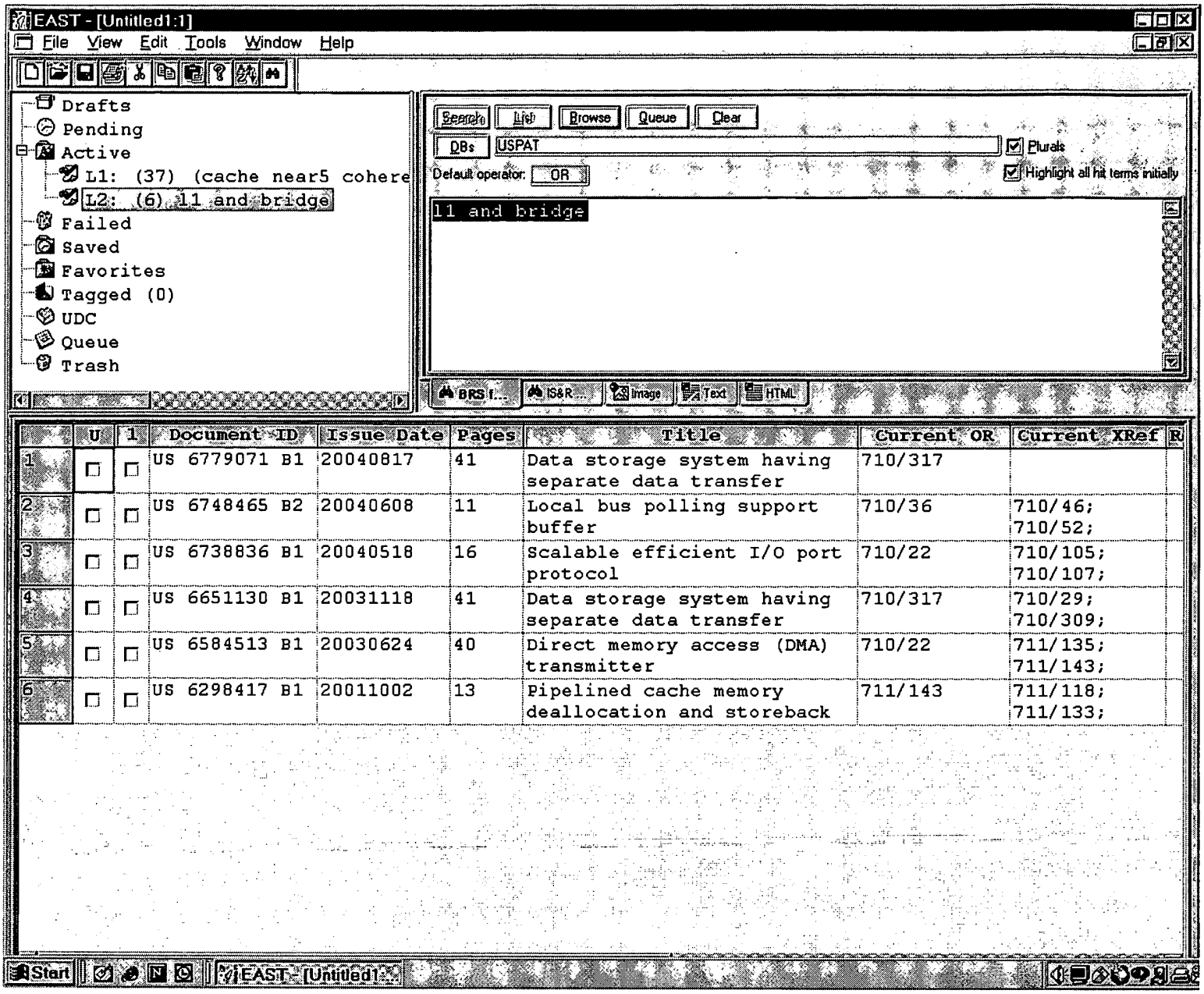
Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L4	l1 and L3	16	L4
L3	710/306,312,112;711/141,148;709/213,214,253;370/401-402;707/201.ccls.	7242	L3
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L2	(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy) same (FIFO or buffer)	3	L2
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy) same (FIFO or buffer)	63	L1

END OF SEARCH HISTORY

h e b b cg b e e ch



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	37	(cache near5 coheren$2 near5 memory) same	USPAT	2004/11/02 13:59			0
2	BRS	L2	6	l1 and bridge	USPAT	2004/11/02 13:59			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 6779071 B1	20040817	41	Data storage system having separate data transfer	710/317		
2	☐	☐	US 6748465 B2	20040608	11	Local bus polling support buffer	710/36	710/46; 710/52;	
3	☐	☐	US 6738836 B1	20040518	16	Scalable efficient I/O port protocol	710/22	710/105; 710/107;	
4	☐	☐	US 6651130 B1	20031118	41	Data storage system having separate data transfer	710/317	710/29; 710/309;	
5	☐	☐	US 6584513 B1	20030624	40	Direct memory access (DMA) transmitter	710/22	711/135; 711/143;	
6	☐	☐	US 6298417 B1	20011002	13	Pipelined cache memory deallocation and storeback	711/143	711/118; 711/133;	

Your search matched **2** of **1088345** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
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cache and coheren* and memory and bridge Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Performance analysis of inclusion effects in multi-level multiprocess caches**
Nelson, B.; Archibald, J.; Flanagan, K.;
Parallel and Distributed Processing, 1991. Proceedings of the Third IEEE Symposium on , 2-5 Dec. 1991
Pages:513 - 516

[Abstract] [PDF Full-Text (272 KB)] **IEEE CNF**

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2 **Scalable Coherent Interface**
Alnaes, K.; Kristiansen, E.H.; Gustavson, D.B.; James, D.V.;
CompEuro '90. Proceedings of the 1990 IEEE International Conference on Computer Systems and Software Engineering , 8-10 May 1990
Pages:446 - 453

[Abstract] [PDF Full-Text (696 KB)] **IEEE CNF**

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Scalable Coherent Interface

Alnaes, K. Kristiansen, E.H. Gustavson, D.B. James, D.V.
Dolphin Server Technol. AS, Oslo, Norway;

This paper appears in: **CompEuro '90. Proceedings of the 1990 IEEE Int Conference on Computer Systems and Software Engineering**

Meeting Date: 05/08/1990 - 05/10/1990
Publication Date: 8-10 May 1990
Location: Tel-Aviv Israel
On page(s): 446 - 453
Reference Cited: 11
Inspec Accession Number: 3842745

Abstract:
The Scalable **Coherent** Interface Project (IEEE P1596) is establishing an inte standard for very-high-performance multiprocessors, supporting a **cache-coh memory** model scalable to systems with up to 64K nodes. The P1596 Scalabl Interface (SCI) will supply a peak bandwidth per node of 1 Gb/s. The SCI sta should facilitate assembly of processor, **memory**, I/O and bus **bridge** cards f multiple vendors into massively parallel systems with throughput far above w possible today. The SCI standard encompasses two levels of interface, a phys and a logical level. The physical level specifies electrical, mechanical and ther characteristics of connectors and cards that meet the standard. The logical-le describes the address space, data transfer protocols, **cache coherence** mec synchronization primitives and error recovery. Logical-level issues such as pa formats, packet transmission, transaction handshake, flow control, and **cache coherence** are addressed

Index Terms:
buffer storage computer interfaces multiprocessing systems standards 1 Gbit/s IE SCI standard Scalable **Coherent** Interface Project address space **cache coherence** mechanisms **cache-coherent-memory** model cards connectors data transfer protc electrical characteristics error recovery flow control interface standard logical level parallel systems mechanical characteristics packet formats packet transmission pe bandwidth physical level synchronization primitives thermal characteristics transact handshake very-high-performance multiprocessors

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Search Results - Record(s) 1 through 3 of 3 returned.

☐ 1. Document ID: NA9406319

Using default format because multiple data bases are involved.

L2: Entry 1 of 3 File: TDBD Jun 1, 1994

TDB-ACC-NO: NA9406319

DISCLOSURE TITLE: Memory Queue Priority Mechanism for a RISC Processor

PUBLICATION-DATA:
IBM Technical Disclosure Bulletin, June 1994, US

VOLUME NUMBER: 37
ISSUE NUMBER: 6A
PAGE NUMBER: 319 - 322

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20030126341 A1

L2: Entry 2 of 3 File: DWPI Jul 3, 2003

DERWENT-ACC-NO: 2003-688504
DERWENT-WEEK: 200365

TITLE: Computer system with improved software to hardware communications has hardware device with cache memory that duplicates portion of FIFO buffer of main memory array and that is kept coherent by way of cache coherency protocol

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: WO 9003002 A, AU 8942117 A, AU 8944083 A, US 4928225 A, US 5029070 A

L2: Entry 3 of 3 File: DWPI Mar 22, 1990

h e b b g e e e f e b ef b e

DERWENT-ACC-NO: 1990-116128
DERWENT-WEEK: 199015

TITLE: Coherent cache structure method in multiprocessor system - ensure that most up-to-date copy is used without storing cache coherency status bits in global memory

Terms	Documents
(cache near5 coheren$2 near5 memory) same (duplicat$3 or copy) same (FIFO or buffer)	3

h e b b g e e e f e b ef b e

Hit List

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Search Results - Record(s) 1 through 10 of 16 returned.

☐ 1. Document ID: US 20030126341 A1

Using default format because multiple data bases are involved.

L4: Entry 1 of 16 File: PGPB Jul 3, 2003

PGPUB-DOCUMENT-NUMBER: 20030126341
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030126341 A1

TITLE: Method and apparatus for eliminating the software generated ready-signal to hardware devices that are not part of the memory coherency domain

PUBLICATION-DATE: July 3, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Bonola, Thomas J.	Magnolia	TX	US	
Larson, John E.	Houston	TX	US	
Olarig, Sompong P.	Pleasonton	CA	US	

US-CL-CURRENT: 710/306

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20030033510 A1

L4: Entry 2 of 16 File: PGPB Feb 13, 2003

PGPUB-DOCUMENT-NUMBER: 20030033510
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030033510 A1

TITLE: Methods and apparatus for controlling speculative execution of instructions based on a multiaccess memory condition

PUBLICATION-DATE: February 13, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Dice, David	Foxborough	MA	US	

US-CL-CURRENT: 712/235; 711/141

h e b b g e e e f e b ef b e

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6742017 B1

L4: Entry 3 of 16 File: USPT May 25, 2004

US-PAT-NO: 6742017
DOCUMENT-IDENTIFIER: US 6742017 B1

TITLE: Data storage system having separate data transfer section and message network with pointer or counters

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 6684268 B1

L4: Entry 4 of 16 File: USPT Jan 27, 2004

US-PAT-NO: 6684268
DOCUMENT-IDENTIFIER: US 6684268 B1

TITLE: Data storage system having separate data transfer section and message network having CPU bus selector

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 5. Document ID: US 6647453 B1

L4: Entry 5 of 16 File: USPT Nov 11, 2003

US-PAT-NO: 6647453
DOCUMENT-IDENTIFIER: US 6647453 B1

TITLE: System and method for providing forward progress and avoiding starvation and livelock in a multiprocessor computer system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 6. Document ID: US 6631447 B1

L4: Entry 6 of 16 File: USPT Oct 7, 2003

US-PAT-NO: 6631447
DOCUMENT-IDENTIFIER: US 6631447 B1

TITLE: Multiprocessor system having controller for controlling the number of processors for which cache coherency must be guaranteed

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b g e e e f e b ef b e

☐ 7. Document ID: US 6581112 B1

L4: Entry 7 of 16 File: USPT Jun 17, 2003

US-PAT-NO: 6581112
DOCUMENT-IDENTIFIER: US 6581112 B1

TITLE: Direct memory access (DMA) receiver

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 8. Document ID: US 6438659 B1

L4: Entry 8 of 16 File: USPT Aug 20, 2002

US-PAT-NO: 6438659
DOCUMENT-IDENTIFIER: US 6438659 B1

TITLE: Directory based cache coherency system supporting multiple instruction processor and input/output caches

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 9. Document ID: US 6304932 B1

L4: Entry 9 of 16 File: USPT Oct 16, 2001

US-PAT-NO: 6304932
DOCUMENT-IDENTIFIER: US 6304932 B1

TITLE: Queue-based predictive flow control mechanism with indirect determination of queue fullness

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 10. Document ID: US 6182176 B1

L4: Entry 10 of 16 File: USPT Jan 30, 2001

US-PAT-NO: 6182176
DOCUMENT-IDENTIFIER: US 6182176 B1
**** See image for Certificate of Correction ****

TITLE: Queue-based predictive flow control mechanism

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L1 and L3	16

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Search Results - Record(s) 11 through 16 of 16 returned.

☐ 11. Document ID: US 6122659 A

Using default format because multiple data bases are involved.

L4: Entry 11 of 16 File: USPT Sep 19, 2000

US-PAT-NO: 6122659
DOCUMENT-IDENTIFIER: US 6122659 A

TITLE: Memory controller for controlling memory accesses across networks in distributed shared memory processing systems

DATE-ISSUED: September 19, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Olnowich; Howard Thomas	Endwell	NY		

US-CL-CURRENT: 709/213; 707/201, 709/214, 711/120

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 12. Document ID: US 6112283 A

L4: Entry 12 of 16 File: USPT Aug 29, 2000

US-PAT-NO: 6112283
DOCUMENT-IDENTIFIER: US 6112283 A

TITLE: Out-of-order snooping for multiprocessor computer systems

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 13. Document ID: US 6044438 A

L4: Entry 13 of 16 File: USPT Mar 28, 2000

US-PAT-NO: 6044438
DOCUMENT-IDENTIFIER: US 6044438 A

TITLE: Memory controller for controlling memory accesses across networks in distributed shared memory processing systems

h e b b cg b cc e

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 14. Document ID: US 5960179 A

L4: Entry 14 of 16 File: USPT Sep 28, 1999

US-PAT-NO: 5960179
DOCUMENT-IDENTIFIER: US 5960179 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus extending coherence domain beyond a computer system bus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 15. Document ID: US 5829033 A

L4: Entry 15 of 16 File: USPT Oct 27, 1998

US-PAT-NO: 5829033
DOCUMENT-IDENTIFIER: US 5829033 A
**** See image for Certificate of Correction ****

TITLE: Optimizing responses in a coherent distributed electronic system including a computer system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 16. Document ID: US 5530933 A

L4: Entry 16 of 16 File: USPT Jun 25, 1996

US-PAT-NO: 5530933
DOCUMENT-IDENTIFIER: US 5530933 A

TITLE: Multiprocessor system for maintaining cache coherency by checking the coherency in the order of the transactions being issued on the bus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L1 and L3	16

h e b b cg b cc e

Display Format: - Change Format

Previous Page Next Page Go to Doc#

h e b b cg b cc e

US-PAT-NO: 6298417

DOCUMENT-IDENTIFIER: US 6298417 B1
See image for Certificate of Correction

TITLE: Pipelined cache memory deallocation and storeback

---------- KWIC ---------

Previous patent

Detailed Description Text - DETX (5):
Computer system 100 typically further includes a first peripheral bus 110 connected to a peripheral port of bus interface unit 104. First peripheral bus 110 is suitably designed in accordance with an industry standard protocol such as the PCI, ISA, or EISA bus protocols to connect with peripheral devices such as peripheral device 120. Peripheral device 120 may comprise, in suitable embodiments, a hard disk controller, a CD controller, a video controller, a graphics accelerator, or various other peripheral devices. A bus bridge 122 provides a path between first peripheral bus 110 and a second peripheral bus 124. A second peripheral bus is frequently incorporated into a computer system 100 to increase the flexibility of computer system 100. In one common arrangement, first peripheral bus 110 complies with the PCI protocol while second bus 124 complies with the ISA standard such that computer system 100 maybe coupled to both PCI and ISA devices.

Detailed Description Text - DETX (9):
A cache miss occurs when processing unit 102 issues an instruction with a system memory address that is not currently reproduced in cache memory subsystem 106. When a miss corresponds to a modified cache, it is necessary to copy the data stored in the cache line to system memory 108 prior to re-writing the cache line with the information required by the cache miss cycle. The copyback process may unnecessarily and undesirably hamper system performance by consuming multiple clock cycles, especially if the cache line size is large relative to cache bus 203. Despite some disadvantages that accompany them, large cache lines are frequently preferred when implementing cache memory arrays to reduce the amount of circuitry required to implement cache tag RAM 206. A copyback of a modified cache line is typically accomplished by copying the line to a buffer or temporary storage location referred to for purposes of this disclosure as a storeback buffer. Accordingly, a preferred embodiment of

(12) **United States Patent**
Chan et al.

(10) **Patent No.: US 6,298,417 B1**
(45) **Date of Patent: Oct. 2, 2001**

(54) **PIPELINED CACHE MEMORY DEALLOCATION AND STOREBACK**

(75) Inventors: **Kin Shing Chan**, Austin; **Dwain Alan Hicks**, Pflugerville; **Michael John Mayfield**; **Shih-Halung Stephen Tung**, both of Austin, all of TX (US)

(73) Assignee: **International Business Machines Corporation**, Armonk, NY (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/196,906**

(22) Filed: **Nov. 20, 1998**

(51) **Int. Cl.**[7] **G06F 12/00**

(52) **U.S. Cl.** **711/143**; 711/118; 711/133; 711/140; 711/159

(58) **Field of Search** 711/133, 134, 711/135, 150, 159, 154, 160, 165, 141, 100, 118, 140, 143

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,526,508	*	6/1996	Park et al.	711/140
5,765,196	*	6/1998	Lienenes et al.	711/143
5,893,151	*	4/1999	Merchant	711/140

* cited by examiner

Primary Examiner—Tuan V. Thai

(74) *Attorney, Agent, or Firm*—Joseph P. Lally; Anthony V. S. England

(57) **ABSTRACT**

A deallocation pipelining circuit for use in a cache memory subsystem. The pipelining circuit is configured to initiate a storeback buffer (SBB) transfer of first line data stored in a first line of a cache memory array if the deallocation pipelining circuit detects a cache miss signal corresponding to the first line and identifies the first line data as modified data. The deallocation pipelining circuit is configured to issue a storeback request signal to a bus interface unit after the completion of the SBB transfer. The circuit initiates a bus interface unit transfer of the first line data after receiving a data acknowledge signal from the bus interface unit. The pipelining circuit is still further configured to deallocate the first line of the cache memory after receiving a request acknowledge signal from the bus interface unit. This deallocation of the first line of the cache memory occurs regardless of a completion status of the bus interface unit transfer whereby a pending fill of the first cache line may proceed prior to completion of the bus interface unit transfer. In one embodiment, the storeback buffer includes first and second segments for storing first and second segment data respectively. In this embodiment, the deallocation pipelining circuit is able to detect the completion of the transfer of the first segment data during the bus interface unit transfer and preferably configured to initiate an SBB transfer of second line data from a second line in the cache memory array in response to the completion of the first segment data transfer. In this manner, the initiation of the second line SBB transfer precedes the completion of the first line bus interface unit transfer.

16 Claims, 4 Drawing Sheets